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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,667	08/29/2003	Katsumi Tsukahara	Q77144	7778

23373 7590 03/29/2006

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EXAMINER	
EHNE, CHARLES	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 03/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,667	TSUKAHARA, KATSUMI	
	Examiner	Art Unit	
	Charles Ehne	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 16-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 16-20 recite 'program product...'. Thus, these claims merely recite a program per se, which is not permissible under the Examination Guidelines for Computers - Related Inventions. The examiner suggests the following as a way to correct those claims: 'A computer program product having a computer readable medium with computer readable program code stored thereon, said computer readable code comprising...'

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8-20 are rejected under 35 U.S.C. 102(b) as being unpatentable by Klug (5,226,152).

As to claim 8, Klug discloses a transaction synchronization control method for use in a fault tolerant computer, said method comprising:

a first step of sending a plurality of, and the same, I/O transactions from a plurality of CPU modules, which process the same instruction string while maintaining clock synchronization, to an I/O module (Figure 1, columns 2-3, lines 66-6); and

a second step of checking if sequences of the received I/O transactions match in each of a plurality of device controllers provided in said I/O module and, if the sequences match, judging that an out-of-synchronization condition is not caused (columns 2-3, lines 66-6 & column 3, lines 53-58).

As to claim 9, Klug discloses a transaction synchronization control method according to claim 8 wherein said second step checks if the sequences of I/O transactions match while waiting for a predetermined time (column 3, lines 53-58).

As to claim 10, Klug discloses a transaction synchronization control method according to claim 9, further comprising a third step of outputting the I/O transactions to said device controller when the sequences match (column 3, lines 45-48, lines 62-66).

As to claim 11, Klug discloses a transaction synchronization control method according to claim 9 wherein, for each device controller, said first step stores the I/O transactions issued from said plurality of CPU modules into a plurality of storage means (column 3, lines 26-28) and

wherein said second step sends the I/O transactions, received from the CPU modules, to comparison means for use in comparing the I/O transactions, checks if the predetermined time has elapsed if the I/O transactions do not match, and judges that an out-of-synchronization condition is not caused if the predetermined time has not yet elapsed (column 3, lines 53-58).

As to claim 12, Klug discloses a transaction synchronization control method according to claim 11 wherein, when the received I/O transactions match, the matching I/O transactions are output to said device controller, one at a time (column 3, lines 45-48, lines 62-66).

As to claim 13, Klug discloses a transaction synchronization control method according to claim 9, further comprising the step of outputting a failure notification when the sequences do not match within the predetermined time (column 3, lines 53-58).

As to claim 14, Klug discloses a transaction synchronization control method according to claim 11, further comprising the step of selecting between said plurality of storage means and said CPU modules as a source when a new I/O transaction is sent to said comparison means (column 3, lines 44-45).

As to claim 15, Klug discloses a transaction synchronization control method according to claim 14 wherein, when the storage means do not contain effective data, said step of selecting between said plurality of storage means and said CPU modules switches the source to the CPU modules (column 3, lines 53-66).

As to claim 16, Klug discloses a transaction synchronization control program product for use in a fault tolerant computer in which the same instruction string is processed by a plurality of CPU modules while maintaining clock synchronization, said program product comprising:

a first step of sending a plurality of, and the same, I/O transactions from the plurality of CPU modules to an I/O module (column 3, lines 26-28); and

a second step of checking if sequences of the received I/O transactions match in each of a plurality of device controllers provided in said I/O module and, if the sequences match; judging that an out-of-synchronization condition is not caused (columns 2-3, lines 66-6 & column 3, lines 53-58).

As to claim 17, Klug discloses a transaction synchronization control program product according to claim 16 wherein said second step checks if the sequences of I/O transactions match while waiting for a predetermined time (column 3, lines 53-58).

As to claim 18, Klug discloses a transaction synchronization control program product according to claim 17, further comprising a third step of outputting the I/O transactions to said device controller when the sequences match (column 3, lines 45-48, lines 62-66).

As to claim 19, Klug discloses a transaction synchronization control program product according to claim 16, further comprising the step of outputting a failure notification when the sequences do not match within the predetermined time or when the sequences of I/O transactions differ (column 3, lines 53-58).

As to claim 20, Klug discloses a transaction synchronization control program product according to claim 17 wherein, for each device controller, said first step comprises the step of storing the I/O transactions, issued from said plurality of CPU modules, into a plurality of storage means (column 3, lines 26-28)

and wherein said second step comprises the steps of sending the I/O transactions received from the CPU modules to comparison means and comparing the I/O transactions; checking if the predetermined time has elapsed if the I/O transactions

do not match; and judging that an out-of-synchronization condition is not caused when the predetermined time has not yet elapsed (column 3, lines 53-58).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klug (5,226,152) taken in view of Suffin (6,691,225).

As to claim 1, Klug discloses a fault tolerant computer comprising:

a plurality of CPU (Central Processing Unit) modules processing the same instruction string while maintaining clock synchronization (Figure 1, columns 2-3, lines 66-6).

Klug discloses an I/O module having a plurality of device controllers each executing input/output control processing for a device (column 2, lines 65-65 & column 3, lines 21-22); and

a transaction synchronization controller, provided in said device controllers, that checks if sequences of I/O transactions issued from said plurality of CPU modules match and, if the sequences match, judges that an out-of-synchronization condition is not caused (Figure 1.2, columns 2-3, lines 66-6 & column 3, lines 53-58).

Klug does not disclose a plurality of I/O modules.

Suffin discloses a redundant, fault tolerant system with redundant central processing units and main memory units that run in "lock step", each processor runs identical copies of the operating system and application programs (column 3, lines 21-31). Suffin does disclose a plurality of I/O modules each having a plurality of device controllers each executing input/output control processing for a device (column 3, lines 32-35).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Suffin's redundant I/O modules in place of Klug's single I/O module. A person of ordinary skill in the art would have been motivated to make the modification because more I/O modules allow the system to control more I/O devices and provide the system an extremely high level of availability to insure uninterrupted operation (Suffin: column 3, lines 18-21 & lines 35-38).

As to claim 2, Klug discloses a fault tolerant computer according to claim 1 wherein said transaction synchronization controller comprises:

timer means for measuring a predetermined time (Figure 2.30, column 4, lines 26-32); and

comparison means for checking if the sequences of I/O transactions, issued from the plurality of CPU modules, match on a device controller basis while waiting for the predetermined time (column 3, lines 53-58).

As to claim 3, Klug discloses a fault tolerant computer according to claim 2 wherein said transaction synchronization controller further comprises an output controller that outputs said I/O transactions to said device controller when said sequences match (column 3, lines 62-66).

As to claim 4, Klug discloses a fault tolerant computer according to claim 3 wherein, when the I/O transactions from the CPU modules match, said output controller outputs the matching I/O transactions to said device controller, one at a time (column 3, lines 45-48, lines 62-66).

As to claim 5, Klug discloses a fault tolerant computer according to claim 2 wherein, when the sequences do not match within the predetermined time or when the sequences of I/O transactions differ, said output controller outputs a failure notification (column 3, lines 53-58).

As to claim 6, Klug discloses a fault tolerant computer according to claim 2, further comprising a plurality of storage means in which the I/O transactions issued from said plurality of CPU modules are stored (column 3, lines 26-28).

As to claim 7, Klug discloses a fault tolerant computer according to claim 2 wherein said transaction synchronization controller further comprises selection circuits

that select between said plurality of storage means and said CPU modules as a source from which I/O transactions to be sent to said comparison means are received (column 3, lines 44-45).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Ehne whose telephone number is (571)-272-2471. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER
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